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Design of Modified Canny Edge Detector Based on FPGA for Portable Device

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Abstract

Edge detection is one of the key stages in image processing and object reorganization. The Canny Edge Detector is one of the most widely used edge detection algorithm due to its superior performance. In this paper, we propose a mechanism to implement the Canny algorithm at the block level without any loss in edge detection performance compared with the original frame-based Canny algorithm. Directly applying the original Canny Edge detection algorithm at the blocklevel leads to excessive edges in smooth regions and to loss of significant edges in high-detailed regions since the original Canny computes the high and low thresholds based on the frame-level statistics. To solve this problem, we present a modified Canny edge detection algorithm that adaptively computes the edge detection thresholds based on the block type and the local distribution of the gradients in the image block. Here we propose the design of modified Canny Edge detection algorithm that results in significantly reduced memory requirement, decrease in latency, increase throughput, with no loss in edge detection performance as compare to original Canny Detector Algorithm. Here we are using matlab to convert image into text/pixel value.

Keyword: Distributed Processing, Canny Edge Detector, High Throughput,, Parallel Processing, FPGA