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Energy Efficient Quaternary Capacitive DAC Switching Scheme for SAR -ADC

Sarvesh S. Chavhan, K. M. Bogawar
[1,2]Electronics Engineering Department, PCE Nagpur, India

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Abstract

This paper presents energy efficient 4-bit successive approximation register analog to digital converter (SAR-ADC) for neural recording front end interface of neural prosthetic system(Brain machine interface). The energy efficient quaternary capacitive switching scheme (QCS) in the implementation of capacitive digital to analog converter (C-DAC) is employed which makes the energy consumption in the C-DAC independent of the output digital code. The proposed quaternary capacitive technique in C-DAC achieves a 50% reduction in the average energy consumption. The design is implemented in 0.25um standard complementary metal-oxide semiconductor technology (CMOS).

Keyword: Neural System, Brain Machine Interface, Switching Scheme, Capacitive DAC, Quaternary Capacitive Switching Scheme, AR-Logic Module, Successive Approximation Registers Analog to Digital Converter, (SARADC)