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Implementation of High Speed Operating FIR Filter with DA Algorithm Comparing Results with MAC Algorithm and Simple FIR Filter Result

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Abstract

Recent years there has been a increasing trend to implement digital signal processing functions in Field Programmable Gate Array (FPGA). therefor, we need to put great effort in designing efficient architectures for digital signal processing functions such as FIR filters, which are widely used in audio and video signal processing, telecommunications etc. We are going to present a method for implementing high speed Finite Impulse Response (FIR) filters using MAC (MULTIPLY AND ACCUMULATE) and Distributed Arithmetic (DA) method. MAC is a conventional FIR filter In these method adders, multipliers and delay elements are used. Distributed Arithmetic (DA) has been used to implement a bit-serial scheme of a general symmetric version of an FIR filter due to its high stability and linearity by taking optimal advantage of the look-up table (LUT) based structure of FPGAs. The performance of the DA technique for FIR filter design is analyzed and the results are compared to the MAC design technique.

Keyword: FIR Filter, DA Algorithm, MAC Algorithn, LUT