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A VERSATILE GENERAL MULTIPLIER-DIVIDER CELL BY USING OPERATIONAL TRANS-RESISTANCE AMPLIFIERS

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Abstract: -

In this paper, we present the design of a versatile general multiplier-divider cell by using the Operational Trans-resistance Amplifier (OTRA) and MOSFETs operating in the linear region. The design and the basic operation of this block is verified. Other operations can also be realized by simply choosing the inputs of the signals at the different terminals. These operations include square root operation, scalar vector multiplier and modulation to name a few. The new cell is reconfigurable and can be programmed by DC voltages. The resulting circuits are simulated by 0.18 m CMOS process through PSPICE. These simulation results verify the versatile operation of this cell.

Keywords: *Multipliers, Dividers, Computational circuits, OTRA*

I. INTRODUCTION

Operational Transresistance Amplifier (OTRA) is one of the basic building blocks in analog circuit design which provides amplification of high frequency signals. OTRA provides a constant bandwidth virtually independent of the gain. Characterized by low input and output impedances, it leads to circuits that are insensitive to stray capacitances, providing current processing at the input terminal which are virtually grounded (Kılınç. S, *et al.* 2007).

The Operational Transresistance Amplifiers has been applied in active filter applications. It has been beneficial in reducing the active element count in filter implementation (Salama, K.N. *et al.* 1999, Chen, J.-J. *et al.* 1995, Chen, J.J., *et al.* 1993) On the other hand the OTRA is not widely used in non-linear circuit applications. For instance, analog multipliers and dividers and other nonlinear functions, have a wide range of applications in many analog signal processing systems, telecommunications and electronic systems. So far, these circuits have been implemented by using OP-Amps, transistor level design, CCTA circuits to name a few techniques (Khachab, N. I. *et al.* 1998, Soliman, A. M. 2008, Tangsrirat, W. 2011, Alikhani, A. *et al.* 2012).

In this paper an OTRA based multiplier-divider block is presented and verified. The circuit uses MOS transistors operating in the linear region. The circuit is reconfigurable to operate as a programmable four-quadrant multiplier or as a programmable divider through the circuit by proper application of the signals.

The effectiveness of the proposed circuits is demonstrated through PSPICE simulation based on 0.18 µm parameters. In Section II, the basic OTRA is presented. The new block parameters and design are presented in section III. The application of the cell as a multiplier/squarer and modulator are discussed in Section IV. The cell as a divider is presented and discussed in Section V. In section VI the operation of the cell as a square-root circuit and as a scalar vector multiplier are discussed. The simulated results are presented in Section VII. Conclusions as well as some comparisons are addressed in Section VIII.

II. THE OTRA CHARACTERISTICS

This section presents the characteristics of the OTRA cell shown in Figure 1. The OTRA is characterized by its low input and output impedances.

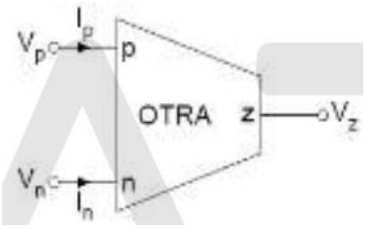

Figure 1: The OTRA Structure and Symbol

The terminal relations between the various voltages and currents are given by Equation (1).

$$\begin{pmatrix} V_P \\ V_n \\ V_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{pmatrix} = \begin{pmatrix} I_P \\ I_n \\ I_z \end{pmatrix} \quad (1)$$

The following equation characterizes the ideal OTRA:

$$V_O = R_m[I_P - I_n] \quad (2)$$

Where: $VP=V_n=0$

If $R_m=\infty$, then $Ip=In$.

III.THE MULTIPLIER-DIVIDER CELL

In this section the proposed versatile cell is discussed and the various relations are derived. The proposed multiplier-divider cell is shown in Figure 2. The circuit consists of an OTRA device and four MOSFETS operating in the linear region. The various signals are applied at the transistors as shown in Figure 2. These signals can be AC, DC or combination of AC or DC signals. Considering the current equation for MOSFET operating in the linear region, one can derive the following equations:

$$I_1 = K_1\left[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2\right] \quad (3)$$

$$I_1 = K_1\left[(X_1 - V_T)Y - Y^2/2\right] \quad (4)$$

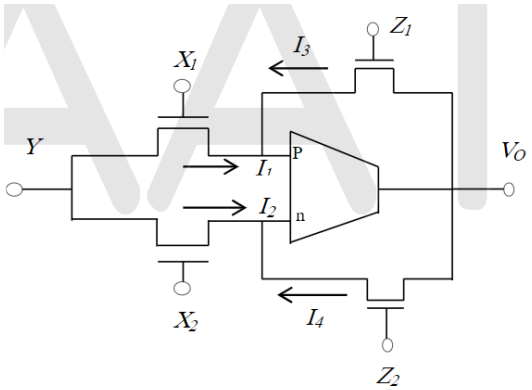

Figure 2: The Multiplier-Divider Structure

Similarly,

$$I_2 = K_2\left[(X_2 - V_T)Y - Y^2/2\right] \quad (5)$$

With

$$K_i = \mu_n C_{OX}\left(W/L\right)_i \quad (6)$$

Where μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit gate area, W is the effective channel width; L is the effective channel length. The other two currents I_3 and I_4 can be verified to be:

$$I_3 = K_3\left[(Z_1 - V_T)V_O - V_O^2/2\right] \quad (7)$$

And,

$$I_4 = K_4\left[(Z_2 - V_T)V_O - V_O^2/2\right] \quad (8)$$

Let $K_1=K_2=K_{in}$,

Then, one can verify that:

$$I_1 - I_2 = K_{in}Y(X_1 - X_2) \quad (9)$$

Let $K_3=K_4=K_O$, Then, one can verify that:

$$I_4 - I_3 = K_O V_O(Z_2 - Z_1) \quad (10)$$

By a node equation at the inputs of the OTRA, then

$$I_1 - I_2 = I_4 - I_3 \quad (11)$$

From equations (9), (10) and (11), it can be shown that:

$$V_O = \frac{K_{in}Y(X_1 - X_2)}{K_O(Z_2 - Z_1)} \quad (12)$$

Let: $(X_1 - X_2) = \Delta X$ and $(Z_2 - Z_1) = \Delta Z$

$$V_O = \frac{K_{in}Y\Delta X}{K_O\Delta Z} \quad (13)$$

If, $X_1 = -X_2 = X$, and $Z_1 = -Z_2 = Z$, then:

$$V_O = \frac{K_{in}YX}{K_O Z} \quad (14)$$

For the MOSFETs to operate in the linear region, the following conditions must be satisfied:

$$Y =\leq \min\left[(X_1 - V_T),(X_2 - V_T)\right] \qquad (15)$$

$$V_O =\leq \min\left[(Z_1 - V_T),(Z_2 - V_T)\right] \qquad (16)$$

It is clear that the circuit realizes the computation of the signals of the form:

$$V = \frac{Y\Delta X}{\Delta Z} \qquad (17)$$

This computational form has many applications in many electronic, telecommunications, computational circuits, and instrumentation circuits to name a few.

IV. THE APPLICATION OF THE CIRCUIT AS A MULTIPLIER/SQUARER/MODULATOR

The circuit block can be configured to operate as a four-Quadrant multiplier by the proper application of the Y, X and Z signals. Let the signals to be applied at the Y and the X inputs, and DC control voltages V_{C1} and V_{C2} at the Z inputs. The expression of Vo is given by equation (18).

$$V_o = \left[\frac{2\left(W/L\right)_i}{\left(W/L\right)_o (V_{C1} - V_{C2})}\right] XY \qquad (18)$$

By this application of DC signals, then the MOSFETs with the Z inputs will operate as a voltage-controlled resistor. The value of this resistor is given by:

$$R = \frac{1}{K_o (V_{C1} - V_{C2})} \qquad (19)$$

Thus, the value of the output is tunable via the DC voltages *VC1* and *VC2*.

4.1 THE APPLICATION OF THE CIRCUIT AS A DIVIDER

The circuit block can be configured to operate as a divider by the proper application of the Y, X and Z signals. DC voltage *VC1* is applied at *X1* and DC voltage of *VC2* is applied at *X2*. At the Z inputs the signals are applied such that Z2=-Z1=z. Let Y=y then the output signal is given by:

$$V_o = \left[\frac{\left(W/L\right)_i (V_{C1} - V_{C2})}{\left(W/L\right)_o}\right] \frac{Y}{Z} \qquad (20)$$

Equation (20) shows that the signal Z is divided. It should be noted that the output voltage is tunable via the DC voltages *VC1* and *VC2*.

THE APPLICATION OF THE CIRCUIT AS A SQUARE-ROOT CIRCUIT,SCALAR VECTOR MULTIPLIER

The circuit block can be configured to operate as a square-root circuit by the proper application of the Y, X and Z signals. The signal for which the square root is needed is applied at the Y input. DC voltage *VC1* is applied at *X1* and DC voltage of *VC2* is applied at *X2*. At the Z inputs the output voltage is applied such that Z2=-Z1=Vo. Then the output voltage is given by the following expression:

$$V_o = \sqrt{\left[\frac{\left(W/L\right)_i (V_{C1} - V_{C2})}{2\left(W/L\right)_o}\right] Y} \qquad (21)$$

The cell can also be operated as a scalar vector multiplier. This is achieved by adding a pair of transistors at the input of the OTRA for each *Xi* and *Yi* signals. The output voltage can be proved to be as:

$$V_O = \alpha \sum_i^n \Delta X_i Y_i \qquad (22)$$

This application of the cell is important in computational circuits. It also can find its applications in neural networks and some convolution circuits.

VII. SIMULATION RESULTS

In this section the performance of OTRA cell configuration is presented. The simulation results of many applications of the cell are presented. These applications include modulator circuit, divider circuit and a squarer circuit. The different circuits were simulated by using PSICE analysis and using the 0.18 µm process. The MOSFETs where matched with (*W/L*=2 *µm*/0.2 *µm*). The simulation results were in good agreement with the theoretical results. The OTRA was simulated with an *Rm* =10M . The different results are shown in Figures 3, 4 and 5.

The results of the cell as a modulator are shown in Figure 3. For this application the signal Y was a 10 KHz sine wave with 0.5 V p-p. A sine wave of 1 KHz frequency was applied at the x inputs

such that X_1=-X_2= X and of 0.5 V p-p. DC voltages were applied at the Z inputs. Where Z_2= 1.5 V, and Z_1=1V. From the figure it is clear that the output signal is modulated as it is supposed to operate.

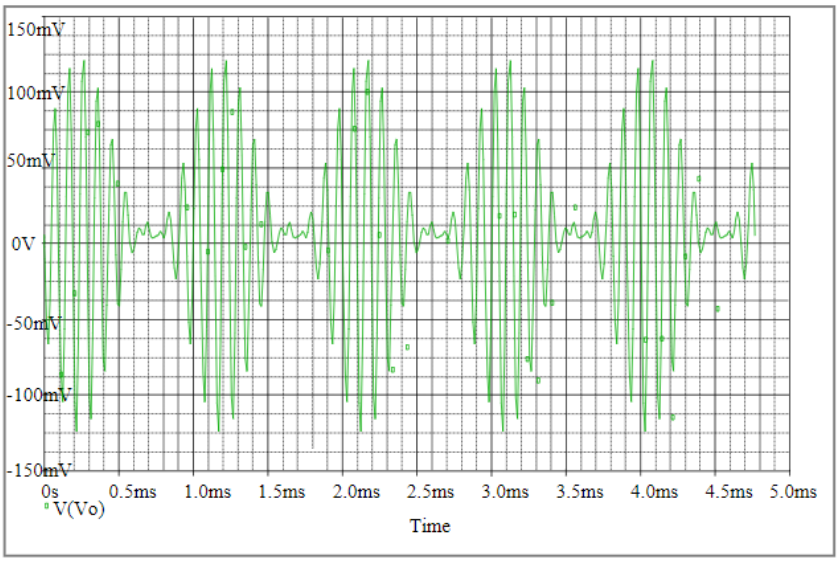

Figure 3: The cell as a modulator circuit

The results of the cell as a modulator are shown in Figure 4. For this application the signal Y was a 10 KHz sine wave with amplitude of 0.5 V p-p. A triangular wave of 1 KHz frequency was applied at the Z inputs such that Z_1=-Z_2= z of 1 V p-p. DC voltage of 0.5 V was applied at the Y input. DC voltages were also applied at the x inputs X_1= 1.5 V, and X_2=1V. From the figure it is clear that the output signal is modulated as it is supposed to operate.

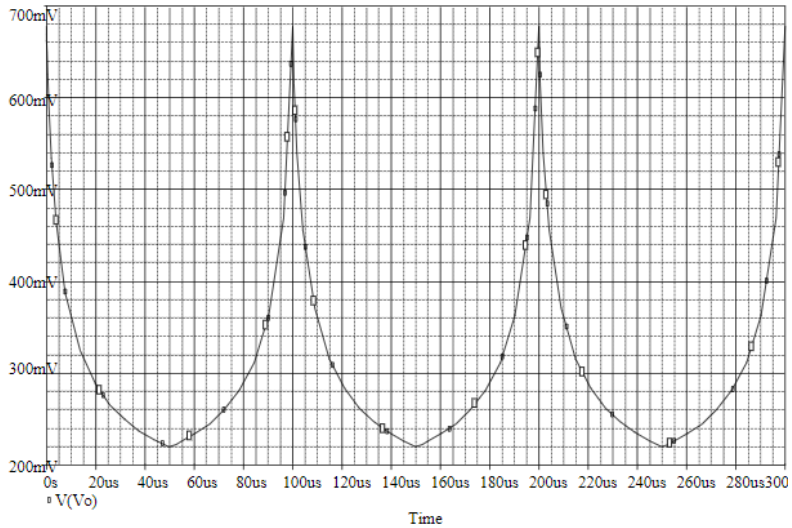

Figure 4: The cell as a divider circuit

The results of the cell as a Squarer are shown in Figure 5. For this application the signal Y was a 1 KHz sine wave with amplitude of 0.5 V p-p. A sine wave of 1 KHz frequency was applied at

the x inputs such that X_1=-X_2= X and of 0.5 V p-p. DC voltages were applied at the Z inputs. Where Z_2= 1.5 V, and Z_1=1V. From the figure it is clear that the output signal is squared as it is supposed to operate.

Figure 5: The cell as a squarer circuit

VIII. CONCLUSIONS

The circuit presented in this paper is simple and versatile. The new cell uses the OTRA and MOSFETs operating in the linear region. This cell can be used to realize different analogue functions. These functions include multiplier, divider, amplitude modulators, squarer circuit, square-foot circuit and scalar vector multiplier. The output of the circuit is programmable via DC control voltages. This will add to the features of the new cell which helps in minimizing the area

and also add to electrical tune-ability feature of the NMOS pair replacing each resistor. Moreover, the cell occupies small chip area. Due to the fact that OTRA is characterized by low output impedance this makes it suitable for cascaded connections. The simulation results prove the operation and the application of the cell. These simulations used the 0.18 µm parameters results show that the cell characteristics are in good agreement with the theory. The operation of the cell can be enhanced in terms of nonlinearity properties of the MOSFETs. This can be achieved by adding an extra pair of transistors which will accommodate X_1, X_2 inputs and Y_1 *and* Y_2 inputs, such that Y_1=-Y_2 =Y. This addition will achieve a complete non-linearity cancellation associated with the MOSFETs.

REFERENCES

[1].Alikhani A., and Ahmadi A., " A novel current-mode four-quadrant CMOS analog multiplier/divider," *International Journal of Electronics and Communications* (AEU), 66, 581- 586, 2012.

[2].Chen J. J., Tsao H.W., Liu S.I., and Chiu W., "Parasitic capacitance insensitive current mode filters using operational transresistance amplifiers". *IEEE proceeding circuit devices systems.* 1995:142:186-92.

[3].Chen J. J., Tsao H.W., Liu S.I., and Tsay J.H., "Design of biquad filters with a single current follower". *IEEE proc circuit devices systems*. 1993:140:165-70.

[4].DURUK A. , GUNES E. O., and Kuntman H., "A new low voltage CMOS differential OTRA for sub-micron technologies", *International Journal of Electronics and Communications* (AEU), 61, (5), 291-299, 2007.

[5].Khachab, N. I., and Ismail M., "MOS multiplier/divider cell for analogue VLSI," *Electronics letter*, Vol. 25, pp. 1550-1551, 1989.

[6].Kılınç S., Keskin A. Ü., and Çam, U, "Cascadable Voltage-Mode Multifunction Biquad Employing Single OTRA". *Frequenz* vol 61, no. 3-4, pp. 84-86, 2007.

[7].Mostafa, H. and Soliman A. M.,"A modified CMOS realization of the operational transresistance amplifier". *Frequenz* vol. 60, pp. 74-76, 2006.

[8].Salama K. N., Solaiman A. M. , "CMOS operational transresistance amplifier for analogue signal processing applications". *Microelectronic J*ournal 1999 ;30:235-245.

[9].Soliman A. M.,"The inverting second generation current conveyors as universal building blocks", *International Journal of Electronics and Communications* (AEU), 62, 114-121, 2008.

[10]. Tangsrirat W., Pukkalanun T., Mongkolwai P. and Surakampontorn W., "Simple current-mode analog multiplier, divider, square-rooter and squarer based on CDTAs", *International Journal of Electronics and Communications* (AEU), 65, 198-203, 2011.